What is claimed is:

1. An error detection system for a memory comprising:

a memory block for storing a data word and a corresponding row parity bit; and

a row parity circuit for receiving the data word and the corresponding row parity bit from the memory block in response to a memory block access operation, the row parity circuit comparing parity of the data word against the corresponding row parity bit for generating an active local parity fail flag in response to parity failure.

2. The error detection system of claim 1, further including a local data I/O circuit for coupling the data word between the memory block and global datalines, and for coupling the corresponding row parity bit between the memory block and the row parity circuit.

3. The error detection system of claim 2, wherein the row parity circuit includes

a serial parity chain for receiving the data word from the local data I/O circuit and for providing a parity output corresponding to parity of the local data, and

a sense circuit for receiving the parity output and the corresponding row parity bit, for providing the active local parity fail flag if the logic state of the parity output and the logic state of the local row parity bit mismatch.

4. The error detection system of claim 3, wherein the serial parity chain includes an even parity line driven to a first logic level at one end thereof, and

an odd parity line driven to a second logic level at one end thereof, the parity output being provided from the other end of the even parity line, and each parity circuit includes cross-over transistors for coupling the parity output to one of the first and second logic levels.

5. The error detection system of claim 4, wherein the sense circuit includes a cross-coupled latch for receiving and latching the parity output, and a comparator circuit for comparing the latched parity output to the local row parity bit.

6. The error detection system of claim 5, wherein the sense circuit includes switching means for coupling the latched parity output to the memory block during a write operation.

7. The error detection system of claim 3, wherein the serial parity chain is segmented into at least two serially connected sub-parity circuits.

8. The error detection system of claim 1, wherein the memory block includes one of redundant rows and columns, and corresponding redundancy circuits.

9. The error detection system of claim 2, further including

a parity block for storing a column parity word, each bit of the column parity word representing column parity for a corresponding bit position of the data word,

a column parity circuit coupled to the local data I/O circuit and the parity block for receiving the data word and the column parity word and for comparing column parity of each bit position of the data word to a corresponding bit of the column parity word in response to the active local parity fail flag, the column parity circuit inverting data of each bit position of the data word that fails column parity.

10. The error detection system of claim 9, wherein the memory block ,the row parity circuit, the parity block and the column parity circuit are integrated in an embedded DRAM.

11. The error detection system of claim 9, wherein the parity block has a configuration identical to that of the memory block, and a parity block data I/O circuit for coupling the word of column parity bits between the parity block and the column parity circuit.

12. The error detection system of claim 10, wherein the column parity circuit includes

a multiplexor circuit coupled between the local data I/O circuit and the global datalines for receiving the bits of the data word and for iteratively providing each bit of the data word to the global datalines,

a parity block multiplexor circuit coupled to the parity block data I/O circuit for receiving the bits of the column parity word and for providing one bit of the column parity word in each iteration,

a parity evaluator circuit coupled to the global datalines for receiving the one bit of the column parity word, the parity evaluator circuit comparing parity of the global datalines to the one column parity bit in each iteration and generating an active global parity fail flag in response to column parity failure, and

a global dataline inverting circuit for receiving and then inverting data of the global datalines in response to the active global parity fail flag.

13. The error detection system of claim 12, wherein the multiplexor circuit and the parity block multiplexor circuit each include a counter for controlling operation thereof.

14. The error detection system of claim 12, wherein the parity evaluator circuit includes

a serial parity chain coupled to the global datalines for providing a parity output corresponding to parity of the global datalines, and

a sense circuit for receiving the parity output and the one bit of the column parity word, for providing the active local parity fail flag if the logic state of the parity output and the logic state of the one bit of the column parity word mismatch.

15. The error detection system of claim 12, wherein the global dataline inverting circuit includes

a flip-flop having an input coupled to one global dataline, an output coupled to a complementary global dataline of the one global dataline, a complementary output coupled to the global dataline, and a clock input for receiving the active global parity fail flag.

16. The error detection system of claim 2, further including a column parity check circuit for selectively inverting bits of the column parity word on the global datalines in a write operation for writing a new word to an address of the data word stored in the memory block, the column parity check circuit including,

a parity comparison circuit for storing the data word and the new word and for comparing each bit position of the stored data word to each corresponding bit position of the stored new word, the parity comparison circuit providing a mismatch flag signal for each bit position having mismatching logic states, and

a parity inverting circuit coupled to the global datalines and for receiving the mismatch flag signals, the parity inverting circuit inverting the logic state of the global datalines in response to the corresponding received mismatch flag signals.

17. The error detection system of claim 1, wherein the memory is a DRAM and the memory block access operation includes a refresh operation.

18. The error detection system of claim 1, wherein the memory is one of an SRAM and an FeRAM, and the memory block access operation includes a data purge operation.

19. A method of detecting and purging bit errors in a memory, comprising:

a) executing a read operation to read a data word and corresponding row parity bit from a memory block of the memory;

b) comparing row parity of the data word against the corresponding row parity bit and generating a row parity fail flag in response to row parity failure;

c) comparing column parity of each bit of the data word against a corresponding bit of a column parity word stored in a parity block of the memory, in response to the row parity fail flag; and,

d) inverting bits of the data word that fail column parity.

20. The method of claim 19, wherein the step of executing includes suppressing the data word from global I/O circuits.

21. The method of claim 19, wherein the step of executing includes providing the data word and the corresponding row parity bit to a local databus.

22. The method of claim 21, wherein the step of comparing row parity includes executing a row parity check of the local databus against the corresponding row parity bit.

23. The method of claim 21, wherein the step of comparing column parity includes iteratively multiplexing bits of the data word from the local databus to a corresponding global dataline in response to row failure.

24. The method of claim 23, wherein the step of comparing column parity includes executing a column parity check of the global datalines against a corresponding column parity bit in each iteration.

25. The method of claim 24, wherein the step of comparing column parity includes inverting the data bits of the global datalines if column parity failure is detected in each iteration.

26. The method of claim 19, wherein the background read operation includes a refresh operation.

27. The method of claim 19, wherein the background read operation includes a data purge operation.

28. The method of claim 25, wherein the step of inverting includes inverting the data bit of a local databus line coupled to one of the global data lines for purging the bit error of the data word stored in the memory block.

29. The method of claim 23, wherein the step of iteratively multiplexing includes selectively activating column access transistors for coupling a different local databus line to the corresponding global dataline in each iteration.

30. The method of claim 29, wherein the step of selectively activating includes incrementing a counter to address and activate a different column access transistor in each iteration.

31. The method of claim 30, further including maintaining activation of the column access transistor corresponding to the memory block having row parity failure.

32. An error detection and purging system for a memory comprising:

a plurality of memory blocks for storing data words and corresponding row parity bits, one of the memory blocks being a parity block for providing a column parity word;

a local data I/O circuit coupled to each memory block for transferring the data words to global datalines;

a row parity circuit coupled to the local data I/O circuit of each memory block for receiving the data words and the corresponding row parity bits in a memory block access

operation, and for comparing parity of the data words against the corresponding row parity bits for generating a corresponding active local parity fail flag in response to row parity failure; and,

a column parity circuit coupled to all the local data I/O circuits, the global datalines, and the parity block for receiving the data words and the column parity word, the column parity circuit iteratively transferring a bit from each of the data words to a different global dataline for comparing parity of the global datalines to a corresponding bit of the column parity word, the column parity circuit inverting data of the global datalines in response to column parity failure in each iteration.

33. The error detection and purging system of claim 32, wherein each row parity circuit includes

a serial parity chain for receiving the data word from the local data I/O circuit and for providing a parity output corresponding to parity of the data word, and

a sense circuit for receiving the parity output and the corresponding row parity bit, for providing the active local parity fail flag if the parity output and the corresponding row parity bit mismatch.

34. The error detection and purging system of claim 33, wherein the serial parity chain includes

an even parity line driven to a first logic level at one end thereof, and

an odd parity line driven to a second logic level at one end thereof, the parity output being provided from the other end of the even parity line, and each parity circuit includes cross-over transistors for coupling the parity output to one of the first and second logic levels.

35. The error detection and purging system of claim 34, wherein the sense circuit includes a cross-coupled latch for receiving and latching the parity output, and a comparator circuit for comparing the latched parity output to the local row parity bit.

36. The error detection and purging system of claim 35, wherein the comparator circuit includes an exclusive OR gate.

37. The error detection and purging system of claim 32, wherein each memory block includes one of redundant rows and columns, and corresponding redundancy circuits.

38. The error detection and purging system of claim 32, wherein the parity block has a configuration identical to that of each memory block, and a parity block data I/O circuit for coupling bits of the column parity word to the column parity circuit.

39. The error detection and purging system of claim 38, wherein the column parity circuit includes

a multiplexor circuit coupled between each local data I/O circuit and the global datalines for receiving the bits of the data word and for iteratively providing each bit of the data word to the global datalines,

a parity block multiplexor circuit coupled to the parity block data I/O circuit for receiving the bits of the column parity word and for providing one bit of the column parity word in each iteration,

a parity evaluator circuit coupled to the global datalines and for receiving the one bit of the column parity word, the parity evaluator circuit comparing parity of the global datalines to the one column parity bit in each iteration and generating an active global parity fail flag in response to column parity failure, and

a global dataline inverting circuit for receiving and inverting data of the global datalines in response to the active global parity fail flag.

40. The error detection system of claim 39, wherein the multiplexor circuit and the parity block multiplexor circuit each include a counter for controlling operation thereof.

41. The error detection and purging system of claim 39, wherein the global dataline inverting circuit includes

a flip-flop having an input coupled to one global dataline, an output coupled to a complementary global dataline of the one global dataline, a complementary output coupled to the one global dataline, and a clock input for receiving the active global parity fail flag.

42. The error detection and purging system of claim 32, further including a column parity check circuit for selectively changing bits of the column parity word on the global datalines in a write operation, for writing a new word to an address of the data word stored in the memory block, the column parity check circuit including,

a parity comparison circuit for storing the data word and the new word and comparing each bit position of the stored data word to each corresponding bit position of the stored new word, the parity comparison circuit providing a mismatch flag signal for each bit position having mismatching logic states, and

a parity inverting circuit coupled to the global datalines and for receiving the mismatch flag signals, the parity inverting circuit inverting the logic state of the global datalines in response to the corresponding received mismatch flag signals.

43. A method for writing row and column parity bits to a memory system in a write operation, the memory system having a memory block for storing a data word and a corresponding row parity bit, and a parity block for storing column parity bits, the method comprising:

a. latching a stored data word read out from an address to which a new data word is to be written;

b. writing the new data word to the address and generating a corresponding row parity bit;

c. comparing data between each bit position of the stored data word and the new word; and,

d. inverting the column parity bits corresponding to mis-matching bit positions.

44. The method of claim 43, wherein the step of latching includes reading the stored data word onto a global databus.

45. The method of claim 43, wherein the step of writing includes latching the new data word.

46. The method of claim 43, wherein the step of inverting includes reading the column parity bits onto a global databus.

47. The method of claim 46, wherein the step of inverting includes inverting the column parity bits of the global databus that correspond to bits of the stored data word that mis-match bits of the new data word.

48. The method of claim 43, further including a memory initialization step prior to the step of latching.

49. The method of claim 48, wherein the memory initialization step includes

i. writing preset logic values to memory cells of an activated wordline,

ii. reading out the preset logic values for latching by bitline sense amplifiers, and

iii. activating all wordlines of the memory block to write the latched preset logic values thereto.

50. The method of claim 49, wherein the step of reading includes disabling bitline precharge and equalize circuits after the preset logic values are latched by the bitline sense amplifiers.

51. The method of claim 49, wherein the step of activating includes iteratively activating individual wordlines.

52. The method of claim 51, wherein the step of iteratively activating individual wordlines includes addressing each wordline with a refresh counter.

53. The method of claim 49, wherein the step of activating includes iteratively activating multiple wordlines simultaneously.

54. The method of claim 49, wherein the step of activating includes simultaneously activating all wordlines.

55. The method of claim 50, wherein the activated wordline includes a master wordline and the step of writing includes activating all column access devices to write the preset logic value to all the memory cells coupled to the master wordline.